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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,683	02/18/2004	Masahiro Kanai	118739	8559

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EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,683	KANAI, MASAHIRO	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10 and 12* is/are rejected.

7)☒ Claim(s) *5-9,11,and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the following communication: the Amendment of February 1, 2006.

2. Claims 1-13 are pending in the case. Claim 1 is an independent claim.

Specification

3. The proposed specification corrections (page 2, line 18) received on February 1, 2006 are approved by Examiner.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Non-volatile memory with two adjacent memory cells sharing same word line.

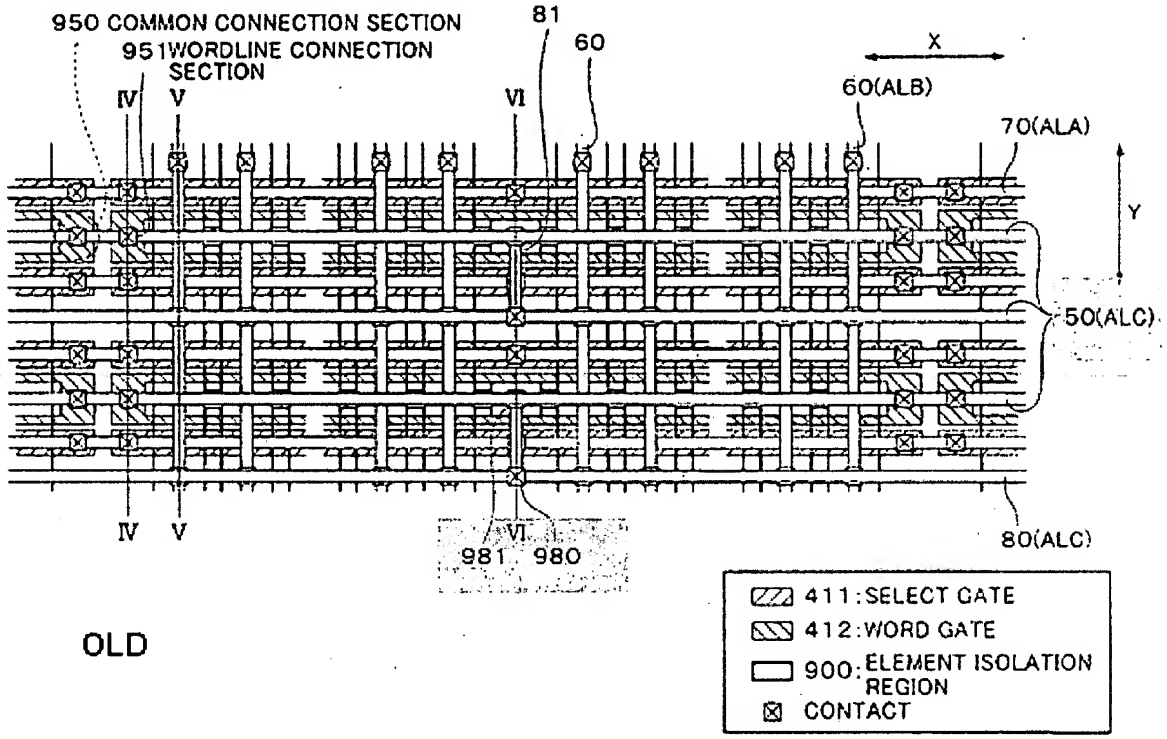
Drawings

5. The proposed drawings corrections (Fig. 3) received on February 1, 2006 are not approved by Examiner.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because three lines extend to 50, of which two are correct; but, the middle extended line should be deleted. Examiner assumes that applicant intended this line on Figure 3 to be labeled "80." Also, it appears that the orientation of "980" and "981" are reversed (see Fig. 3 with respect to Fig. 6).

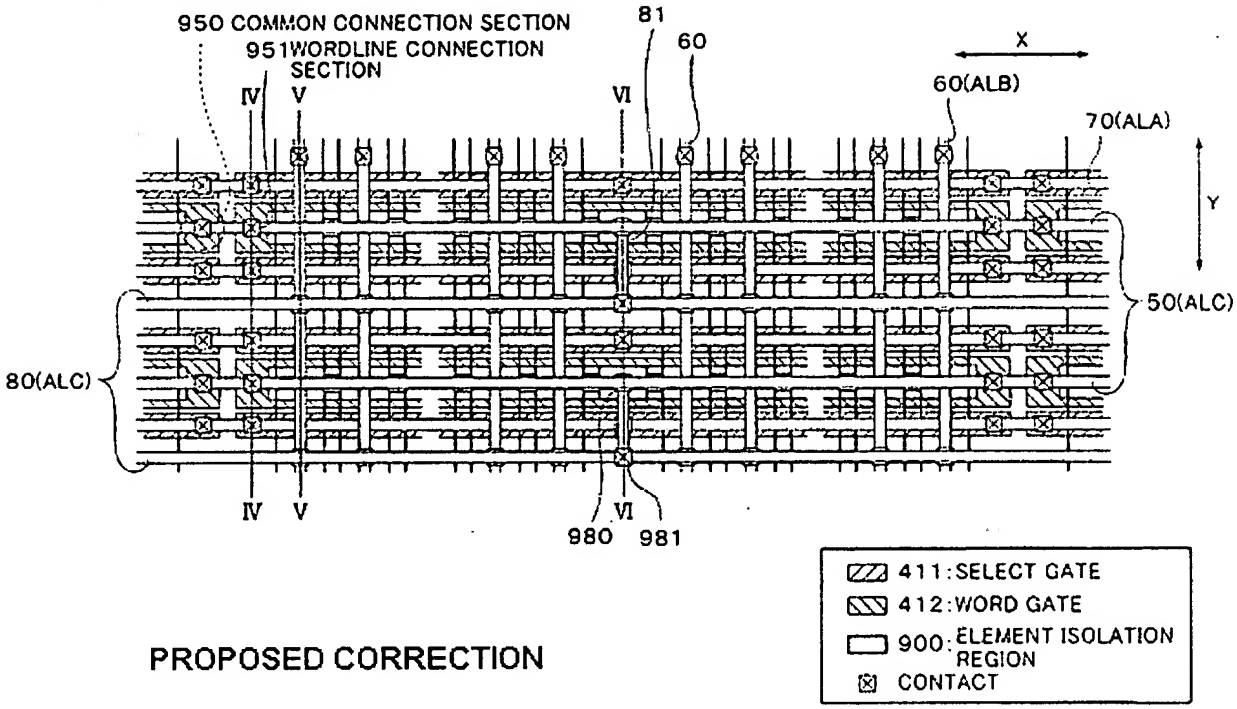
For clarity purposes, Examiner provides the following proposed correction to Figure 3 (reversing order of 980 and 981; and correcting line 50):

FIG. 3



OLD

FIG. 3



PROPOSED CORRECTION

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

7. It appears that Applicant overlooked the previously set forth obviousness-type double-patenting of claims 1, 3, and 4 over Owa (U.S. Patent Application Publication 2004/0229407) which stands as reproduced below.

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. **Claims 1, 3, and 4 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, and 5 of copending Owa (U.S. Patent Application Publication 2004/0229407).** Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications similarly claim a non-volatile memory device comprising memory cells with impurity layers, element isolation regions, word gates and select gates, word line connection sections, word gate interconnects, and common connection sections.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding independent claim 1, Owa's claim 1 recites a non-volatile semiconductor memory device comprising: a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction; a plurality of element isolation regions; wherein each of the memory cells includes one of the source line diffusion layers (**SDL**; a first impurity layer), one of the bitline diffusion layers (**BDL**; a second impurity layer), a channel region between the SDL (first impurity layer) and BDL (second impurity layer), a word gate and a select gate which are disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region; wherein a plurality of word gate wiring layers (word line connection section) is connected with at least one word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section) which is connected in common with two adjacent word gates above at least one of the element isolation regions.

Regarding independent claim 3, Owa's claim 1 further recites memory cells with word gates in the memory array arranged in a column direction and a row direction. Word lines are well-known in the art to be oriented in a row direction and to be connected to word gates. Thus, the word-gates, which are connected to the word lines, are arranged in the row direction forming word-gate rows. Owa's claim 1 further recites that each of the word gate common connection sections (common connection sections) is connected in common with the two adjacent word gates over at least one element

isolation region. Owa's claim 5 recites that the word gate common connection sections (common connection sections) are arranged along the column direction.

Regarding independent claim 4, Owa's claim 1 further recites a plurality of word gate wiring layers (word line connection section) is connected with at least one word gate interconnection (word gate interconnect) which is connected with one of the word gate common connection sections (common connection section).

10. **Claims 1, 3, and 4 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 4 of Natori (U.S. Patent 6,898,120). Although the conflicting claims are not identical, they are not patentably distinct from each other because:**

Regarding independent claim 1, Natori claim 1 and claim 4 recite similar limitations of instant application's claim 1: first region, source, drain, and word lines that are commonly connected with word gates. Natori claim 1 and claim 4 do not explicitly recite limitations of instant application's claim 1: element isolation regions, a first impurity layer, a second impurity layer, and a first word line connection section.

However, to one of ordinary skill in the art at the time the invention was made, it would be understood that: an element isolation region is met by a first region as recited in Natori claim 4, a first and second impurity layer is met by a source and drain as recited in Natori claim 1, and a word line connection section connecting a plurality of word gate interconnects disposed over the element isolation region is met by word lines

commonly connected with word gates wherein the word gate is disposed over the first region as recited in Natori claim 4.

Regarding independent claim 3, Natori claim 1 and 4 recite similar limitations including: a plurality of word lines each which is commonly connected with the word gates of the memory cells in each row wherein each of the unit word line driver sections drives two of the word lines connected respectively to two word gates adjacent in the column direction, and a first region. Natori claim 1 and 4 do not explicitly recite a plurality of common connection sections, each of the common connection sections connecting two of the word-gate rows adjacent in the column direction over the element isolation regions.

However, to one of ordinary skill in the art at the time the invention was made, it would be understood that: a common connection section connecting two of the word gate rows adjacent in the column direction is met by a plurality of word line driver sections driving two of the word lines connected respectively to two word gates adjacent in the column direction as recited in Natori claim 1, and a word line connection section connecting a plurality of word gate interconnects disposed over the element isolation region is met by word lines commonly connected with word gates wherein the word gate is disposed over the first region as recited in Natori claim 4.

Regarding independent claim 4, Natori claim 1 recites similar limitations including: a unit word line driver section, word lines, and word lines commonly connected with word gates wherein the unit word line driver connects two adjacent word gates. Natori claim 1 does not explicitly recite: a first word line connection section

connecting at least one of the word gate interconnects with one of the common connection sections.

However, to one of ordinary skill in the art at the time the invention was made, it would be understood that: a first word line conection section is met by the unit word line driver section, the common connection section is met by the the word lines each of which is commonly connected with the word gates, and the word gate interconnect is met by the word lines as recited in Natori claim 4.

11. **Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 10 of copending Maemura (U.S. Patent Application Publication 2004/0228181). Although the conflicting claims are not identical, they are not patentably distinct from each other because:**

Regarding independent claim 1, Maemura '181 claim 1 and claim 10 recite similar limitations of instant application's claim 1: first region, source, drain, and word lines that are commonly connected with word gates. Maemura '181 claim 1 and claim 10 do not explicitly recite limitations of instant application's claim 1: element isolation regions, a first impurity layer, a second impurity layer, and a first word line connection section.

However, to one of ordinary skill in the art at the time the invention was made, it would be understood that: an element isolation region is met by a first region as recited in Maemura '181 claim 10, a first and second impurity layer is met by a source and drain

as recited in Maemura '181 claim 1, and a word line connection section connecting a plurality of word gate interconnects disposed over the element isolation region is met by word lines commonly connected with word gates wherein the word gate is disposed over the first region as recited in Maemura '181 claim 1 and claim 10.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. **Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Ogura et al. (U.S. Patent 6,759,290).** Ogura et al. show a nonvolatile semiconductor memory device comprising a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction (see Fig. 6E).

Ogura et al. show the memory cell array includes a plurality of element isolation regions (Fig. 10A [302]).

Ogura et al. show each of the memory cells includes a first and second impurity layers (Fig. 4A [103]) and a channel region located between the diffusion regions (not explicitly labeled), and a word gate (Fig. 4A [140]) and a select gate (Fig. 4A [142]) disposed to face the channel region (not explicitly labeled), and a nonvolatile memory element formed between the word gate and channel region (see Fig. 4A).

Ogura et al. show a first word line connection section (Fig. 10C [365]), which connects at least one plurality of word gate interconnects (Fig. 10C [381]) with at least one of the word gates (Fig. 10A [340]), is disposed over at least one of the element isolation regions (Fig. 10A [302]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima et al. (U.S. Patent 6,069,824) in view of Ogura et al. (U.S. Patent 6,759,290).

Regarding independent claim 1, Kojima et al. show a memory cell array (Fig. 2 [10]) in which a plurality of memory cells are arranged in a row direction and a column direction (column 2, lines 34-36). Kojima et al. show schematic diagrams of the memory cells that include control gate, floating gate, and source and drain (first and

second impurity layer; see column 3, lines 4-7); however, Kojima et al. are silent with respect to the structural limitations of the memory cells, which include: a plurality of element isolation regions; a channel region located between the diffusion regions, and a word gate and a select gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and channel region; and a first word line connection section, which connects at least one plurality of word gate interconnects with at least one of the word gates, is disposed over at least one of the element isolation regions.

Ogura et al. show the memory cell array includes a plurality of element isolation regions (Fig. 10A [302]); each of the memory cells includes a first and second impurity layers (Fig. 4A [103]) and a channel region located between the diffusion regions (not explicitly labeled), and a word gate (Fig. 4A [140]) and a select gate (Fig. 4A [142]) disposed to face the channel region (not explicitly labeled), and a nonvolatile memory element formed between the word gate and channel region (see Fig. 4A); and a first word line connection section (Fig. 10C [365]), which connects at least one plurality of word gate interconnects (Fig. 10C [381]) with at least one of the word gates (Fig. 10A [340]), is disposed over at least one of the element isolation regions (Fig. 10A [302]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ogura et al. to the teachings of Kojima et al. such that the memory cells of Kojima et al. have the structural limitations of Ogura et al. for the purpose of implementing "stiched" or "strapped" word lines in order to reduce word line resistance. Further motivation to perform the above stated modification is evidented by

the fact that both Kojima et al. and Ogura et al. show non-volatile memories in an array structure and have similar classification in class 365 (static memories).

Regarding dependent claim 2, Kojima et al. disclose that it is well-known in the art that flash memory collectively is capable of erasing data on a predetermined block (Fig. 2 [BK0-BKm]) basis (Kojima et al. column 1, lines 9-11).

Regarding dependent claim 10 and 12, Kojima et al. show the memory cell array (Fig. 2 [10]) includes at least one source interconnect (Fig. 2 [SL0-SLm]) and a plurality of first source line connection sections (Fig. [connection from SL0 to unlabeled S/D of B00]) wherein each of the first source line connections sections (see Fig. [connection from SL0 to unlabeled S/D of B00]) connects the source interconnect (Fig. 2 [SL0-SLm]) to an impurity layer (Fig. 2 [unlabeled S/D of B00]).

Response to Arguments

14. Applicant's arguments, see page 4 section IV, filed February 1, 2006 with respect to art rejection of claims 1-13 over Natori have been fully considered and are persuasive. The rejection of claims 1-13 over Natori has been withdrawn.

15. The terminal disclaimer filed on February 1, 2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 10/782,975 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

16. **Claims 5-9, 11, and 13 are objected to as being dependent upon a rejected base claim**, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

With respect to dependent claim 5, there is no teaching or suggestion in the prior art to the memory described in claim 1 with further limitations of a common connection section connecting two of the word-gate rows adjacent in the column direction over one of the element isolation regions on which the first word line connection section is disposed.

With respect to dependent claim 6, there is no teaching or suggestion in the prior art to the memory described in claim 1 and claim 3 with further limitations of a plurality of common connection sections connecting two of the word-gate rows adjacent in the column direction over one of the element isolation regions on which the first word line connection section is disposed.

With respect to dependent claim 11 and 13, there is no teaching or suggestion in the prior art to the source interconnects include a third interconnect extending along the row direction, and a fourth interconnect extending along the column direction and wherein at least on of the first source line connections sections includes a second

source line connection section which connects the third interconnect with the fourth interconnect.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs. A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)). Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through Private PAIR·only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

Tuan T. Nguyen

NOT APPROVED
AGS
2/15/2006

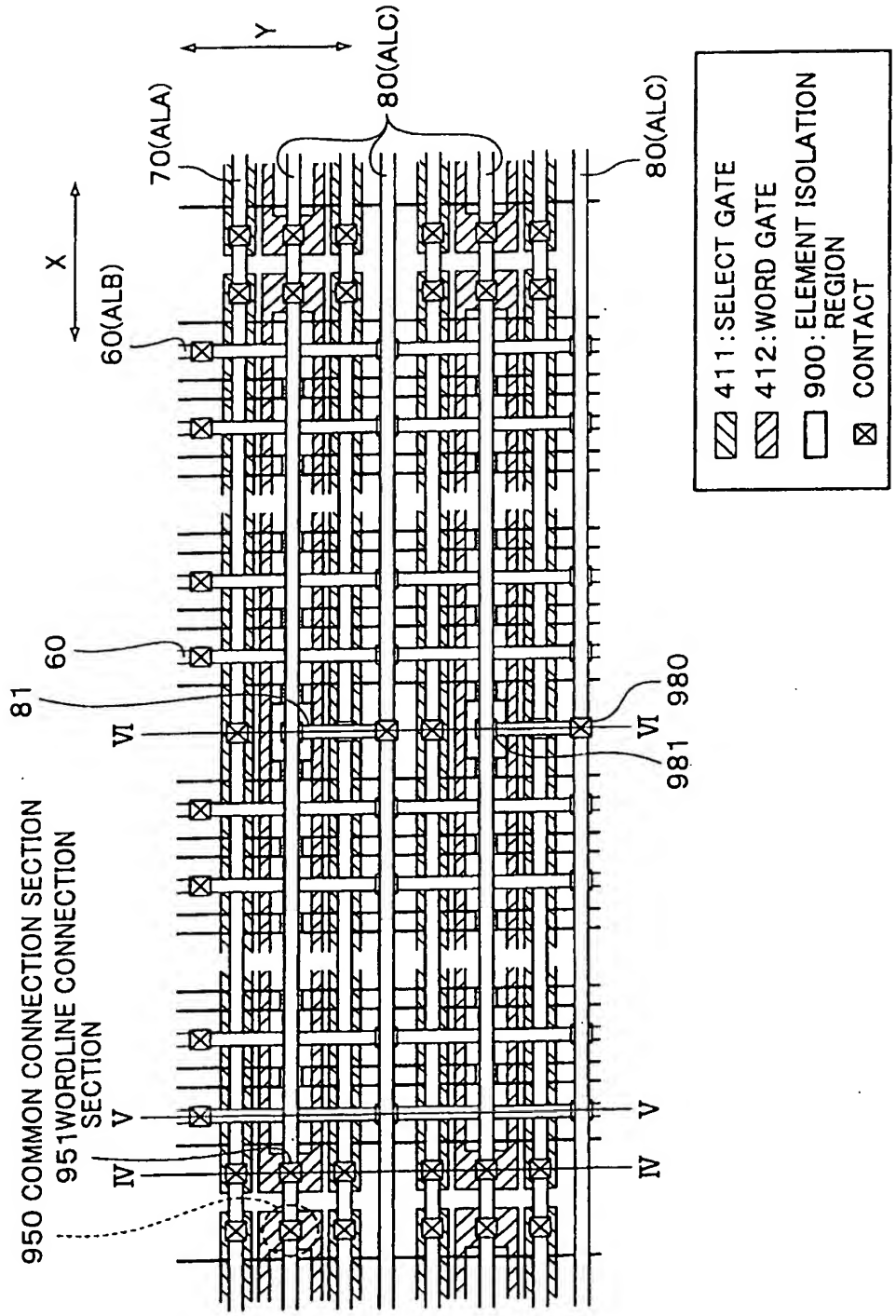


FIG. 3